

What is claimed is:

1. A packaging structure for back-to-back chips, including:
 - a substrate;
 - 5 a first chip, having an active side and an inactive side, and the active side of the first chip partially combining with the substrate and conducted with the substrate by wire-bonding;
 - 10 a second chip, having an active side and an inactive side, and the inactive side of the second chip combining with the inactive side of the first chip, while the active side of the second chip conducted with the substrate by wire-bonding; and
 - 15 an encapsulation, covering the first chip and the second chip for protecting the packaging structure for back-to-back chips.
2. The packaging structure for back-to-back chips as recited in claim 1, wherein the combination between the first chip and the substrate is made by the adhesion manner of an adhesion layer.
3. The packaging structure for back-to-back chips as recited in claim 1, wherein the combination between the second chip and the first chip is made by the adhesion manner of an adhesion layer.
4. The packaging structure for back-to-back chips as recited in claim 1, 20 wherein the first chip and the second chip are the chips with same size.
5. The packaging structure for back-to-back chips as recited in claim 1, wherein the first chip and the second chip are the chips with different size.
6. The packaging structure for back-to-back chips as recited in claim 1, wherein the first chip and the second chip are the chips with same function.
- 25 7. The packaging structure for back-to-back chips as recited in claim 1, wherein the first chip and the second chip are the chips with different function.
8. The packaging structure for back-to-back chips as recited in claim 1, 30 wherein arranged plural solder balls are on the substrate and the packaging structure for back-to-back chips is coupled with a circuit board by the solder

balls.

9. A packaging process for back-to-back chips as claim 1, comprising following steps:

- a) providing a first chip, a second chip and a substrate, wherein the first chip and the second chip having an active side and an inactive side respectively;
- b) combining the active side of the first chip partially with the substrate;
- c) conducting the active side of the first chip to the substrate by wire-bonding;
- d) combining the inactive side of the second chip with the inactive side of the first chip;
- e) conducting the active side of the second chip to the substrate by wire-bonding.

10 15 20 25 30 35 40 45 50 55 60 65 70 75 80 85 90 95 100 105 110 115 120 125 130 135 140 145 150 155 160 165 170 175 180 185 190 195 200 205 210 215 220 225 230 235 240 245 250 255 260 265 270 275 280 285 290 295 300 305 310 315 320 325 330 335 340 345 350 355 360 365 370 375 380 385 390 395 400 405 410 415 420 425 430 435 440 445 450 455 460 465 470 475 480 485 490 495 500 505 510 515 520 525 530 535 540 545 550 555 560 565 570 575 580 585 590 595 600 605 610 615 620 625 630 635 640 645 650 655 660 665 670 675 680 685 690 695 700 705 710 715 720 725 730 735 740 745 750 755 760 765 770 775 780 785 790 795 800 805 810 815 820 825 830 835 840 845 850 855 860 865 870 875 880 885 890 895 900 905 910 915 920 925 930 935 940 945 950 955 960 965 970 975 980 985 990 995 1000 1005 1010 1015 1020 1025 1030 1035 1040 1045 1050 1055 1060 1065 1070 1075 1080 1085 1090 1095 1100 1105 1110 1115 1120 1125 1130 1135 1140 1145 1150 1155 1160 1165 1170 1175 1180 1185 1190 1195 1200 1205 1210 1215 1220 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7225 7230 7235 7240 7245 7250 7255 7260 7265 7270 7275 7280 7285 7290 7295 7300 7305 7310 7315 7320 7325 7330 7335 7340 7345 7350 7355 7360 7365 7370 7375 7380 7385 7390 7395 7400 7405 7410 7415 7420 7425 7430 7435 7440 7445 7450 7455 7460 7465 7470 7475 7480 7485 7490 7495 7500 7505 7510 7515 7520 7525 7530 7535 7540 7545 7550 7555 7560 7565 7570 7575 7580 7585 7590 7595 7600 7605 7610 7615 7620 7625 7630 7635 7640 7645 7650 7655 7660 7665 7670 7675 7680 7685 7690 7695 7700 7705 7710 7715 7720 7725 7730 7735 7740 7745 7750 7755 7760 7765 7770 7775 7780 7785 7790 7795 7800 7805 7810 7815 7820 7825 7830 7835 7840 7845 7850 7855 7860 7865 7870 7875 7880 7885 7890 7895 7900 7905 7910 7915 7920 7925 7930 7935 7940 7945 7950 7955 7960 7965 7970 7975 7980 7985 7990 7995 8000 8005 8010 8015 8020 8025 8030 8035 8040 8045 8050 8055 8060 8065 8070 8075 8080 8085 8090 8095 8100 8105 8110 8115 8120 8125 8130 8135 8140 8145 8150 8155 8160 8165 8170 8175 8180 8185 8190 8195 8200 8205 8210 8215 8220 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15. The packaging structure for back-to-back chips as recited in claim 9, wherein the first chip and the second chip are the chips with same function.

16. The packaging structure for back-to-back chips as recited in claim 9, wherein the first chip and the second chip are the chips with different function.

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